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presence of the gate definition spacer controls the final junction geometry by establishing the lateral extent of the implanted volume and by limiting the available diffusion paths for the implanted species during anneal.

In comparing the length of channel **25** in FIG. **2C** to the length of channel **35** of FIG. **3C**, it can be seen that the length of channel **35** is shorter. The shorter channel length improves the frequency response of the device since the carrier transit time is reduced.

FIG. **4** shows the p-n junction interface geometry associated with the conventional structure of FIG. **2C**. For purposes of comparison, the interface length can be approximated as the sum of three line segments of length r and two arc segments of length $\pi r/2$. The effective length for the junction interface is thus approximately $(3+\pi)r$, or $6.14r$. In this example, the length r is approximately equal to the diffusion distance associated with the anneal step, which is the same for both FIG. **2C** and FIG. **3C**.

FIG. **5** shows the p-n junction interface geometry associated with the structure of FIG. **3C** of the present invention. In comparison to FIG. **4**, the p-n junction interface length consists of two line segments of length r and one arc segment of length $\pi r/2$, giving an effective length for the junction interface of approximately $(2+\pi/2)r=3.57r$. The effective junction interface length of the present invention is thus about 40% less than that of a conventional structure.

Since the parasitic capacitances C_{gs} and C_{gd} are dependent on the junction interface length, it can be seen that the present invention offers a significant reduction in overall parasitic capacitance in comparison to a conventional structure at a given channel width. The reduction in capacitance attributable to C_{gs} and C_{gd} can be approximated by examining the reduction in interface length on the source side of the channel and the drain side of the channel.

In FIG. **4**, the source side length taken from the channel midpoint **40** is $(\pi+1)r/2=2.07r$, whereas in FIG. **5** the source side length taken from the channel midpoint **50** is $r/2=0.5r$. Thus, C_{gs} is reduced by approximately 75%.

In FIG. **4**, the drain side length taken from the channel midpoint **40** is $(\pi+5)r/2=4.07r$, whereas in FIG. **5** the source side interface length taken from the channel midpoint **50** is $(\pi+3)r/2=3.07r$. Thus, C_{gd} is reduced by approximately 25%.

FIG. **6** shows another embodiment of the present invention that provides a further reduction in C_{gd} . After the annealed structure of FIG. **3C** has been fabricated, an additional trench etch is performed to remove a portion of the post-anneal gate region. The walls of this gate surface reduction trench **61** are approximately aligned with the surface of the gate definition spacers **36**. In comparison with the conventional structure of FIG. **4**, a reduction from $4.07r$ to $2.07r$ is obtained in the drain side interface length from channel midpoint **40**. This amounts to an approximate 50% reduction in C_{gd} . The gate surface reduction trench **61** as shown has the minimum depth required to achieve a reduction in C_{gd} , (e.g. a portion of the p-n junction has been removed and the depletion region removed with it). A further reduction in fringing capacitance can be achieved by increasing the depth of the second trench **61** beyond that shown in FIG. **6**.

FIG. **7** shows the structure of FIG. **6** with an oxide backfill **70**. Backfill of the trenches provides a surface that is available for contact metallization. Alternatively, contacts to the gate regions **34** may be established in portions of the trench.

FIG. **8** shows an overall process flow **200** in accordance with the present invention. In the first step **210** a trench is etched in a semiconductor substrate. In the second step **215**

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a gate definition spacer is deposited on the walls of the trench etched in the first step. In the third step **220** a gate region is implanted. In the fourth step **225** the gate region is annealed. In the fifth step **230** a second trench is etched to remove a portion of the gate volume. In the sixth step **235** the trench is backfilled with oxide.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

The invention claimed is:

1. A JFET comprising:

a gate definition spacer adjacent to a corresponding trench wall surface, wherein said corresponding trench wall surface defines one side of a trench previously formed in a substrate, said trench comprising a bottom surface adjacent to said substrate, wherein said corresponding trench wall surface forms a boundary between said gate definition spacer and a source region adjacent to said gate definition spacer; and

an implanted gate region formed below said bottom surface of said trench, wherein said implanted gate region comprises at least one rounded p-n junction interface formed at a corner of said implanted gate region due to annealing, wherein said implanted gate region extends laterally such that at least a segment of the rounded p-n junction interface closest to the trench wall surface is substantially co-planar with said corresponding trench wall surface and a channel width of a channel region for said JFET is approximately equal to a width of said source region between trench walls of said JFET.

2. The JFET of claim 1 wherein said JFET is an n-channel JFET.

3. The JFET of claim 2 wherein said JFET is an enhancement mode JFET.

4. The JFET of claim 2 wherein said JFET is a depletion mode JFET.

5. The JFET of claim 1 wherein said JFET is a p-channel JFET.

6. The JFET of claim 5 wherein said JFET is an enhancement mode JFET.

7. The JFET of claim 5 wherein said JFET is a depletion mode JFET.

8. A JFET comprising:

a gate definition space adjacent to a corresponding trench wall surface, wherein said corresponding trench wall surface defines one side of a trench previously formed in a substrate, said trench comprising a bottom surface adjacent to said substrate, wherein said corresponding trench wall surface forms a boundary between said gate definition spacer and a source region; and

an implanted gate region formed below said bottom surface of said trench, wherein said implanted gate region comprises at least one rounded p-n junction interface formed at a corner of said implanted gate region due to annealing, wherein said implanted gate region extends laterally such that at least a segment of